Computer Instruction-Set Design and Implementation
DUAL 2-way SUPERSCALAR CORES, and SHARED MEMORY

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EGR/CS 433 Advanced Computer Engineering Final Lab Project

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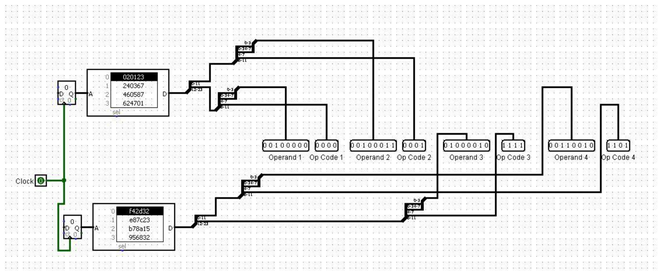
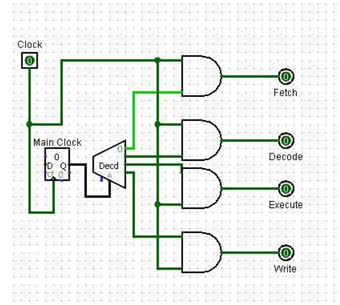


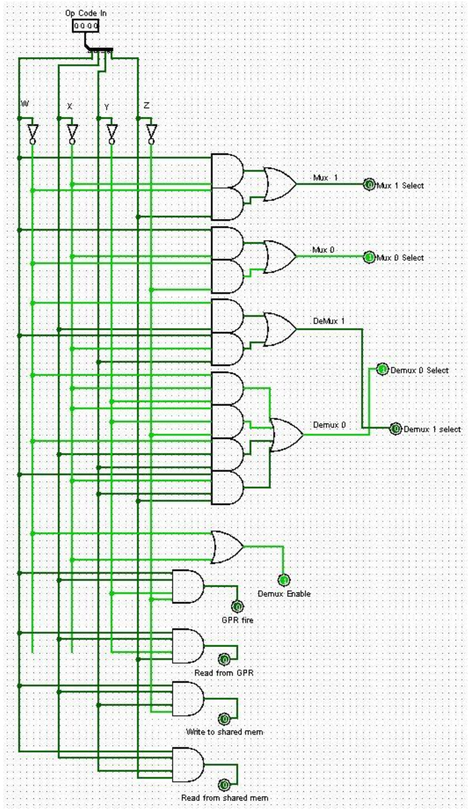
Finite State Machine and Stack



Clock and States

Instruction Set

- (OP-CODE = 0000) Add Immediate Data to counter #1 (UP-COUNTER)
- (OP-CODE = 0001) Add Immediate Data to counter #2 (DOWN-COUNTER)
- (OP-CODE = 0010) Compare Immediate Data with counter #1 (UP-COUNTER)
- (OP-CODE = 0011) Compare Immediate Data with counter #2 (DOWN-COUNTER)
- (OP-CODE = 0100) AND Immediate Data to counter #1 (UP-COUNTER)
- (OP-CODE = 0101) AND Immediate Data to counter #2 (DOWN-COUNTER)
- (OP-CODE = 0110) OR Immediate Data to counter #1 (UP-COUNTER)
- (OP-CODE = 0111) OR Immediate Data to counter #2 (DOWN-COUNTER)
- (OP-CODE = 1000) Add Counters
- (OP-CODE = 1001) Compare Counters
- (OP-CODE = 1010) AND Counters
- (OP-CODE = 1011) OR Counters
- (OP-CODE = 1100) Write Accumulator to General Purpose Register shared by pipelined data paths (Pipeline #1 has priority)
- (OP-CODE = 1101) Read from General Purpose Register shared by pipelined data paths. Make next instruction uses this for OPERAND #1
- (OP-CODE = 1110) During WAIT STATE , Write Accumulator to SHARED MEMORY– just one fixed location (CORE1,Pipe1 has priority)
- (OP-CODE = 1111) During WAIT STATE , Read from SHARED MEMORY. Make next instruction use this for OPERAND #1



Control Logic

Design Goals

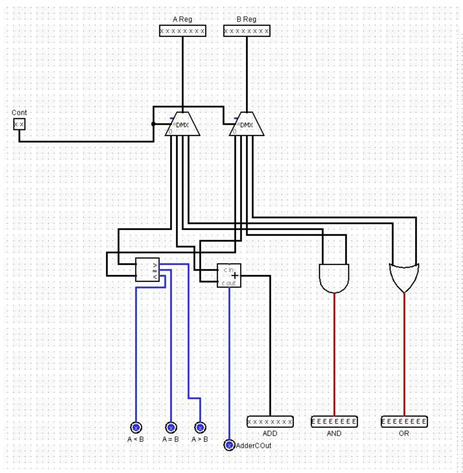
1) Use Logisim, and everything in the past labs, including two SUPERSCALAR pipelines with Buffer-Register/Latches at the beginning of each pipelined data path, Accumulator Buffer-Register/Latches at the end of each pipelined data path, a FINITE MACHINE for the machine instruction cycle (FETCH, DECODE, EXECUTE, WAIT), and one shared General Purpose Register. This will all be one CORE.

2) Duplicate everything in another CORE

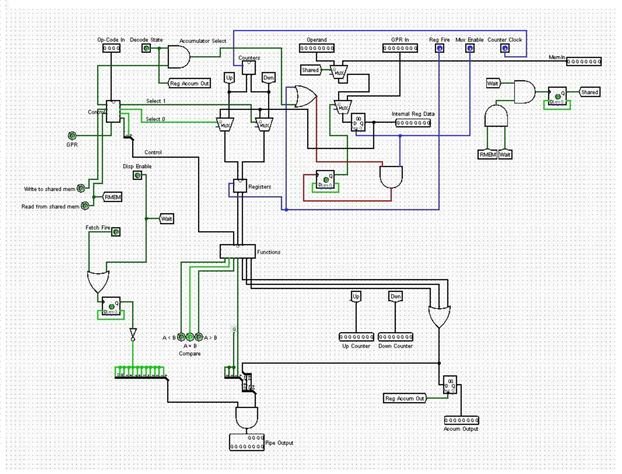
3) Add a SHARED MEMORY (RAM) for the CORES to share data through IPC (Inter-Processor Communication)

4) Implement the two new instructions OP- CODE=1110 and OP-CODE=1111 in each CORE using the WAIT STATE of pipelines

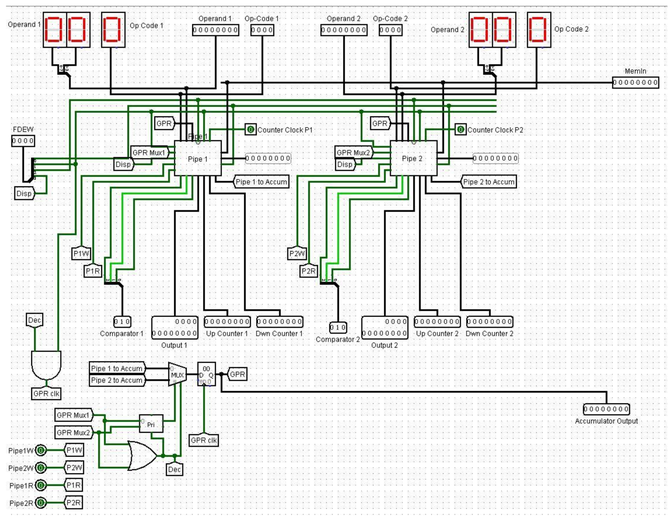
5) Create a non-exhaustive testing methodology to show the full functioning of your DUAL-CORE SMP 2-WaySuperScalar computer



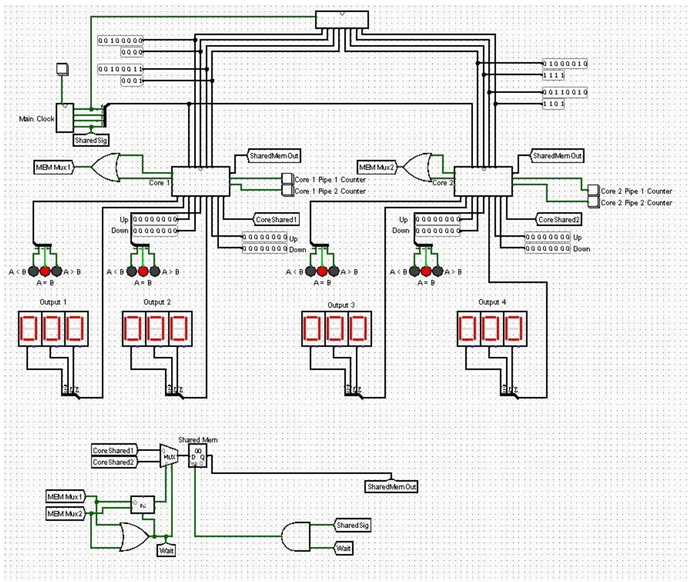
Functions



Pipe



Core



Main